UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/515,376	02/29/2000	Sandeep Bhutani	30454-00243(LSI C4-4247)	1883

24319 7590 04/10/2003

LSI LOGIC CORPORATION
1621 BARBER LANE
MS D-106, LEGAL DEPARTMENT
MILPITAS, CA 95035

EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2123	7

DATE MAILED: 04/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/515,376	Bhutani et al.
Examiner	**Art Unit**
Thai Phan	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Feb. 29, 2000*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-22* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is response to patent application S/N: 09/515,376. Claims 1-22 are pending in this Office Action.

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-22 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-15 of U.S. Patent No. 6,484,297. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are directed to method and system for computing delays of a cell in an integrated circuits. The cell delay computation is based on process variation parameters, temperature parameters, operation voltage, input ramptime, and load capacitance. They are presented in the claims in the manners that are minor variation obvious to each others.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jetton et al., US patent no. 6,028,995.

As per claim 1, Jetton discloses method and system for computing delays of a cell in an integrated circuit with feature limitations substantially similar to the claimed invention. According to Jetton, the method includes steps of

generating a first set of the delays of the cell by assigning nominal values to the cell parameters (col. 6, line 20 to col. 7, line 24, col. 10, lines 35-48, col. 11, lines 58-65, col. 12, lines 1-23),

generating a second set of the delays of the cell by varying values assigned to the parameters of the cell (col. 6, line 20 to col. 7, line 24, col.. 10, lines 9-34),

creating a delay equation based on the first and second set of the delays (col. 6, line 4 to col. 7, line 24, col. 10, lines 8-34) and for deriving derating factor for various circuit operation conditions,

and calculating cell delay using the delay equation, wherein the delay equation characterizes the delays in terms of the parameters of the cell (cols. 9-10). Jetton does not expressly disclose parameters such as process variation, temperature, supply voltage related to the cell for delay characterization.

Practitioner in the art at the time of the invention was made would have found Jetton disclosure of cell operation under normal and best/worst case, and derating factor for scaling delay characterization in various operations would obviously imply cell parameters such as supply voltage, process variation, and temperature because such parameters are related to the cell operation.

As per claim 2, Jetton discloses normal mode of cell operation (col. 10, lines 1-49) would obviously imply the limitations of setting cell parameters to nominal values.

As per claim 3, Jetton discloses varying input ramptime in deriving derating factor for the delay characterization.

As per claim 4, Jetton discloses best/worst ramptime which could include a minimum input ramptime and a maximum allowable ramptime,

As per claim 5, Jetton discloses best/worst load capacitance including a minimum allowable and maximum allowable capacitance load as claimed.

As per claim 6, Jetton discloses varying process to a non-nominal process for worst and best analysis.

As per claims 7 and 8, Jetton discloses non nominal circuit operation which could implies varying temperature and supply voltage to non nominal values to analyze worst and best case conditions (col. 10, lines 17-34)..

As per claims 9-10, Jetton discloses varying ramptime and load capacitance as claimed (col. 3, lines 18-25, col. 6, lines 28-34, cols. 8-9).

As per claim 11-12, Jetton discloses delay equations are generated as function of circuit operation parameters such as power supply, operating temperature, process variation, capacitance load, etc.

As per claim 13, Jetton discloses method and system for computing delays of a cell in an integrated circuit with feature limitations substantially similar to the claimed invention. According to Jetton, the method includes steps of

generating a first set of the delays of the cell by assigning nominal values to the cell parameters (col. 6, line 20 to col. 7, line 24, col. 10, lines 35-48, col. 11, lines 58-65, col. 12, lines 1-23),

assigning a time value within a first range to an input ramptime of the cell during the generation of each of the delay in the first set for normal operation (col. 7, lines 25-30, col. 10, line 9-12, for example),

assigning a load value to an output load of the cell also in normal condition (col. 7, lines 41-57, col, 10, lines 9-12),

generating a second set of the delays of the cell in a second simulation by using non-nominal values of the circuit operation parameters (col. 10, lines 8-34),

creating a delay equation based on the first and second set of the delays (col. 6, line 4 to col. 7, line 24, col. 10, lines 8-34) and for deriving derating factor for various circuit operation

and calculating cell delay using the delay equation, wherein the delay equation characterizes the delays in terms of the parameters of the cell (cols. 9-10). Jetton does not expressly disclose parameters such as process variation, temperature, supply voltage related to the cell for delay characterization.

Practitioner in the art at the time of the invention was made would have found Jetton disclosure of cell operation under normal and best/worst case, and derating factor for scaling delay characterization in various operations would obviously imply cell parameters such as supply voltage, process variation, and temperature because such parameters are related to the cell operation.

As per claim 14, Jetton discloses assigning time value within the first range to the input ramptime of the cell (col. 7, line 12 to col. 9, line 67), and load value within the second range (cols. 7-9).

As per claims 15-16, Jetton discloses generating delay equation with coefficients which is function of circuit operation parameters such as process variation, nominal operating temperature, power supply, capacitive load, ramptime, etc. (Evaluation of Model Parameters, cols. 7-9), and inserting such generated coefficients into the delay equations for cell delay analysis.

As per claims 17 and 18, claims 17 and 18 are directed to the same apparatus in order to perform steps of generating delay equation in a circuit cell.

Jetton discloses method and system for computing delays of a cell in an integrated circuit with feature limitations substantially similar to the claimed invention. According to Jetton, the apparatus includes a electronic design automation tools including processor (col. 1, last paragraph) for executed stored program for generating delay equation in the EDA, memory in the design tools for storing program instructions for performing steps of

generating a first set of the delays of the cell by assigning nominal values to the cell parameters in circuit normal operating conditions (col. 6, line 20 to col. 7, line 24, col. 10, lines 35-48, col. 11, lines 58-65, col. 12, lines 1-23),

assigning a time value within a first range to an input ramptime of the cell during the generation of each of the delay in the first set for normal operation (col. 7, lines 25-30, col. 10, line 9-12, for example),

assigning a load value to an output load of the cell also in normal condition (col. 7, lines 41-57, col, 10, lines 9-12),

generating a second set of the delays of the cell in a second simulation by using non-nominal values of the circuit operation parameters (col. 10, lines 8-34),

creating a delay equation based on the first and second set of the delays (col. 6, line 4 to col. 7, line 24, col. 10, lines 8-34) and for deriving derating factor for various circuit operation

and calculating cell delay using the delay equation, wherein the delay equation characterizes the delays in terms of the parameters of the cell (cols. 9-10). Jetton does not expressly disclose parameters such as process variation, temperature, supply voltage related to the cell for delay characterization.

Practitioner in the art at the time of the invention was made would have found Jetton disclosure of cell operation under normal and best/worst case conditions, and derating factor for scaling delay characterization in various operations would obviously imply cell parameters such as supply voltage, process variation, and temperature because such parameters are related to the cell operation. Claims 17-18 are thus rejected in like manner.

As per claim 19, claim 19 is directed to the same apparatus in order to perform steps of generating delay equation in a circuit cell. Jetton discloses method and system for computing delays of a cell in an integrated circuit with feature limitations substantially similar to the claimed invention. According to Jetton, the apparatus includes a electronic design automation tools including processor (col. 1, last paragraph) for executed stored program for generating

delay equation in the EDA, memory in the design tools for storing program instructions for performing steps of

generating a first set of the delays of the cell by assigning nominal values to the cell parameters (col. 6, line 20 to col. 7, line 24, col. 10, lines 35-48, col. 11, lines 58-65, col. 12, lines 1-23),

assigning a time value within a first range to an input ramptime of the cell during the generation of each of the delay in the first set for normal operation (col. 7, lines 25-30, col. 10, line 9-12, for example),

assigning a load value to an output load of the cell also in normal condition (col. 7, lines 41-57, col, 10, lines 9-12),

generating a second set of the delays of the cell in a second simulation by using non-nominal values of the circuit operation parameters (col. 10, lines 8-34),

creating a delay equation based on the first and second set of the delays (col. 6, line 4 to col. 7, line 24, col. 10, lines 8-34) and for deriving derating factor for various circuit operation

and calculating cell delay using the delay equation, wherein the delay equation characterizes the delays in terms of the parameters of the cell (cols. 9-10). Jetton does not expressly disclose parameters such as process variation, temperature, supply voltage related to the cell for delay characterization.

Practitioner in the art at the time of the invention was made would have found Jetton disclosure of cell operation under normal and best/worst case, and derating factor for scaling delay characterization in various operations would obviously imply cell parameters such as

supply voltage, process variation, and temperature because such parameters are related to the cell operation. Claim 19 is thus rejected in like manner.

As per claim 20, Jetton discloses assigning time value within the first range to the input ramptime of the cell (col. 7, line 12 to col. 9, line 67), and load value within the second range (cols. 7-9).

As per claims 21-22, Jetton discloses generating delay equation which is function of circuit operation parameters such as process variation, nominal operating temperature, power supply, capacitive load, ramptime, etc. (Evaluation of Model Parameters, cols. 7-9). Jetton also discloses generating a set of coefficients for the delay equation, including inserting such coefficients into delay equation for cell delay analysis.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 5,274,568, issued to Blinne et al., on Dec. 1993

2. US patent no. 5,692,160, issued to Sarin, Harish, on Nov. 1997

3. US patent no. 5,896,299, issued to Ginetti et al., on Apr. 1999

4. US patent no. 6,038,384, issued to Ehrler, Timothy, on Mar. 2000

5. US patent no. 6,090,152, issued to Hayes et al., on July 2000

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239, (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Thaiphan
Patent Examiner
AU 2123

April 7, 2003